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(71) Applicant: APPLIED MATERIALS, INC. [US/US]; 3050 Bowers Avenue, Santa Clara, CA 95054 (US).

(72) Inventors: SMARGIASSI, Eugene; 6148 Dunn Avenue, San Jose, CA 95123 (US). WHITE, Anthony, F.; 20061 Forest Avenue, Cupertino, CA 95014 (US). PEUSE, Bruce, W.; 27 Cobblestone Lane, San Carlos, CA 94070 (US). HOGAN, Finbarr, J.; Apartment 302, 400 Riverside Court, Santa Clara, CA 95054 (US). AHMAD, Wayez, R.; 2213 Stratford Drive, Milpitas, CA 95035 (US).

(74) Agents: BERNADICOU, Michael, A. et al.; Blakely, Sokoloff, Taylor & Zafman LLP, 17th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US).

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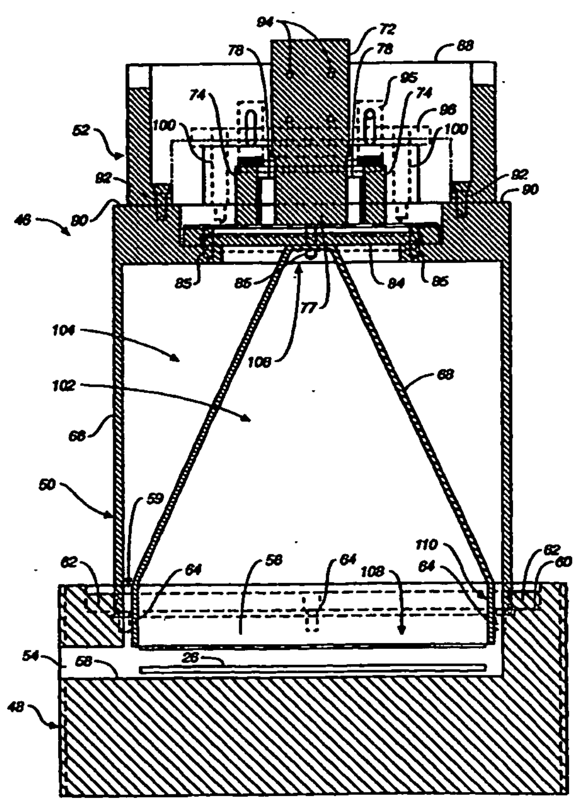
(57) Abstract

During a rapid thermal process, fragments can break away from a wafer and fall onto a temperature sensor in the process chamber. The wafer fragments can compromise the accuracy of the temperature signals generated by sensor probes. In particular, the fragments can attenuate or otherwise interfere with the radiation received from the wafer. This interference can undermine the accuracy of the temperature measurement signal generated by the probes. If the temperature control function is compromised, excessive temperature gradients can result in damage to the wafer, reducing device yield and degrading device quality. To alleviate the effects of wafer fragments, the presence of a wafer fragment is detected. An image acquisition device acquires an image of a wafer. A processor analyses the acquired image to determine whether a wafer fragment is present. The processor analyzes the acquired image for optical density contrast changes indicative of the presence of a wafer fragment. Detection of a wafer fragment allows the rapid thermal process to be stopped so that the fragment can be cleared away prior to insertion of the next wafer into the deposition process chamber.



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DETECTION OF WAFER FRAGMENTS IN A WAFER PROCESSING APPARATUS

The present invention relates to wafer processing and, more particularly, to systems and methods for quality control in a wafer process.

A variety of techniques are available for processing of wafers to fabricate semiconductor devices. Rapid thermal processing (RTP), for example, is widely used in semiconductor fabrication applications in which rapid temperature cycling is necessary or desirable. Examples of common rapid thermal processing applications include annealing, oxidation, and nitridation. A rapid thermal processing chamber typically includes a housing with a support for a wafer to be processed, one or more heat sources, such as lamps, that generate radiation to heat the wafer, and a reflector plate that forms a reflective cavity for more effective heating.

Temperature uniformity is a critical factor in the quality of the rapid thermal process. Different areas of the wafer can exhibit different energy absorption or emissivity characteristics. Moreover, the spatial heating profile of the heat source can be somewhat nonuniform. Consequently, the rapid thermal process can produce significant thermal gradients across the surface of the wafer. Excessive thermal gradients can result in structural damage to the wafer, directly impacting device yield and quality. With flood lamp heat sources, it is often difficult to control cross-substrate temperature. With zoned heat sources, however, temperature can be spatially controlled to more effectively minimize thermal gradients across the wafer.

For spatial control of cross-wafer temperature, particularly with zoned heat sources, a rapid thermal processing chamber typically incorporates a temperature sensing device. The temperature sensing device may include, for example, an array of temperature sensor probes such as pyrometers. The temperature sensing device senses the temperature of the wafer, often at several positions, during the heating cycle.

Temperature signals generated by the temperature sensing device are processed to generate control signals for the heat source.

Accordingly, the accuracy of the temperature signals provided by the temperature sensing device is important for effective control of the heat source, and therefore is a significant factor in device fabrication quality and yield. Any inaccuracies in the temperature measurement can undermine the effectiveness of the temperature control function, opening the door for temperature gradients that can damage the wafer being processed.

SUMMARY

The present invention is directed to a system and method for detecting wafer fragments in a wafer processing apparatus. The system and method can be useful in maintaining the accuracy of the temperature control function of a wafer deposition process. In particular, the system and method facilitate the detection of wafer fragments in a deposition processing chamber. Such wafer fragments can adversely affect the accuracy of temperature measurements within the chamber.

The system and method are particularly useful in controlling the quality of a rapid thermal process given the stringent temperature requirements of such a process. The system and method may find ready application, however, in a variety of wafer processes in which the presence of fragments is a concern, and therefore are not limited to rapid thermal processing. Nevertheless, for purposes of illustration, reference will be made to the characteristics of the rapid thermal process in describing certain exemplary embodiments of the present invention.

During a rapid thermal process, fragments can break away from the wafer and fall onto the temperature sensing device, or onto surfaces between the device and the wafer such as the reflector plate. The wafer fragments can compromise the accuracy of the temperature signals generated by the temperature sensing device. With pyrometer probes, for example, wafer fragments can fall onto the reflector plate

at positions generally coincident with the probes. The wafer fragments can attenuate or otherwise interfere with the infrared radiation received from the wafer.

This interference can undermine the accuracy of the temperature measurement signal generated by the probes, and ultimately degrade the temperature control function across the surface of the wafer. If the temperature control function is ineffective, excessive temperature gradients can result in damage to the wafer, reducing device yield and degrading device quality. Also, the effects of the wafer fragment can persist for subsequent wafers processed within the rapid thermal process chamber unless the fragment is cleared away, e.g., from the reflector plate.

To alleviate the effects of wafer fragments, in accordance with an embodiment of the present invention, the potential presence of a wafer fragment over a temperature sensing device such as an array of probes is detected. The presence of a wafer fragment can be detected, for example, using machine vision techniques. An image acquisition device acquires an image of at least a portion of a wafer that is processed by the rapid thermal process chamber. The image can be acquired following removal of the wafer from the rapid thermal process chamber, and receipt of the wafer into a viewing chamber. The viewing chamber can form part of a subsequent process station, such as a cooling chamber. The acquired image is analyzed to detect the absence of a portion of the wafer. This absence is indicative of fragmentation and the potential presence of a wafer fragment within the rapid thermal process chamber

As an example, the wafer can be analyzed for optical contrast between the wafer surface and missing portions of the wafer. In particular, during imaging, the wafer can be set against an illuminated background that provides back-illumination for the wafer. Optical contrast between the wafer surface and the illuminated background provides an indication of the absence of a portion of the wafer, and thus the potential presence of a wafer fragment on the temperature measurement device or some surface between the wafer mount and the temperature measurement device.

Optical density contrast can be detected by analyzing the optical densities of pixels in the wafer image and comparing the densities to a target density range. Once a number of neighboring pixels exhibiting the requisite density range are detected, the size of the area defined by the pixels can be analyzed. For example, the size of the pixel area can be compared to another threshold value corresponding to a fragment size that could be detrimental to the temperature measurement function.

Detection of a wafer fragment allows the rapid thermal process to be stopped so that the fragment can be cleared away from the rapid thermal process chamber. For example, upon detection of a wafer fragment, an advisory can be generated. The advisory may serve as the basis for automated removal of the fragment, or as a notification to a human operator for manual intervention.

By removing the fragment, a potential source of error in the temperature measurement generated by the temperature sensing device can be eliminated before the next wafer is processed. In this manner, the accuracy of the temperature measurement can be maintained, thereby avoiding processing problems with subsequent wafers in the process run. The result is a reduced probability of excessive temperature gradients that can lead to device yield and quality deficiencies.

In one embodiment, the present invention provides a system for analysis of a wafer for the absence of wafer fragments, the system comprising a viewing chamber, a wafer support member disposed within the chamber, a background surface disposed adjacent the wafer support member within the viewing chamber, an illumination source that directs illuminating radiation toward a wafer positioned on the wafer support member, and an image acquisition device oriented to acquire an image representative of at least a portion of the wafer from a side of the wafer support member opposite the background surface.

In another embodiment, the present invention provides a system for detecting the presence of a wafer fragment in a deposition process chamber, the system comprising an illumination source that provides a pattern of illuminating radiation about an edge of a wafer processed within the chamber, an image acquisition

device oriented to acquire an image representative of at least a portion of a surface of the wafer, wherein the illumination source provides back-illumination for the edge of the wafer, and processor that analyzes the acquired image to detect the absence of a portion of the wafer, and generates an advisory in the event the absence of a portion of the wafer is detected.

In a further embodiment, the present invention provides a method for detecting the presence of a wafer fragment in a deposition process chamber, the method comprising illuminating an area adjacent an edge of a wafer processed within the chamber with a pattern of radiation, acquiring an image representative of at least a portion of the wafer set against a background surface, wherein the pattern of radiation provides back-illumination for the edge of the wafer, analyzing the acquired image to detect the absence of a portion of the wafer, and generating an advisory in the event the absence of a portion of the wafer is detected.

In an added embodiment, the present invention provides a system for analysis of a wafer for the absence of wafer fragments, the system comprising a viewing chamber, a wafer support member disposed within the chamber, an illumination source disposed adjacent a first side of the wafer, the illumination source generating illuminating radiation about an edge portion of the wafer, and an image acquisition device oriented to acquire an image representative of at least a portion of a wafer positioned on the wafer support member from a side of the wafer support member opposite the illumination source.

In a further embodiment, the present invention provides a system for analysis of a wafer for the absence of wafer fragments, the system comprising a viewing chamber, a wafer support member disposed within the chamber, a background surface disposed adjacent the wafer support member within the viewing chamber, an image acquisition device oriented to acquire an image representative of at least a portion of a wafer positioned on the wafer support member from a side of the wafer support member opposite the background surface, an illumination source that projects illuminating radiation within the viewing chamber, an illumination shield

disposed within the viewing chamber, the illumination shield defining an interior region and an exterior region, wherein the illumination shield is oriented such that the illuminating radiation is substantially restricted to the exterior region and a field of view of the image acquisition device is substantially restricted to the interior region, and the exterior region is arranged such that the illuminating radiation illuminates a portion of the background surface adjacent an edge of the wafer to thereby provide back-illumination for the edge of the wafer.

A wafer image can be analyzed, in each of the above embodiments, by identifying an optical density contrast change, and determining whether a portion of the wafer is absent based on identification of the optical density contrast change. In particular, analysis may involve identifying a contrast area having an optical density that contrasts with a target range of optical density, estimating a size of the contrast area, comparing the estimated size to a threshold value, and indicating detection of the absence of a portion of the wafer in the event the estimated size exceeds the threshold value.

If the image is acquired with the wafer set against a background surface, the target range of optical density may correspond to a range associated with the background surface. Further, the background surface can be illuminated. In one embodiment, the background surface can be illuminated adjacent an edge portion of the wafer to thereby provide back-illumination for the wafer. An illumination shield serves to substantially prevent incidence of the illumination radiation on a top surface of the wafer, thereby better preserving any optical contrast for analysis. In another embodiment, the illumination source can be disposed on a side of the wafer adjacent the background surface.

The edge portion of the wafer is most likely to produce wafer fragments. Accordingly, if desired, analysis can be limited to the edge portion. In this case, missing portions of the wafer edge will exhibit sharp optical contrast with the wafer due to the presence of the illuminated background surface, which will be visible

through the fragmented area. At the same time, image processing overhead can be minimized.

In addition to analyzing optical density contrast, the size of a contrast area can be estimated to estimate the size of a potential wafer fragment. The estimated size can be compared to a threshold size indicative of the size of a wafer fragment that potentially could have an effect on the temperature measurement and control functions. As an example, the size of a contrast area can be estimated in terms of the number of image pixels exhibiting the requisite contrast. The pixel count then can be compared to a threshold pixel count. If the size exceeds the threshold, an advisory can be generated. In response to the advisory, the operation of the rapid thermal process chamber can be halted automatically or by manual intervention.

Other advantages, features, and embodiments of the present invention will become apparent from the following detailed description and claims.

DESCRIPTION OF DRAWINGS

FIG. 1 is cross-sectional side view illustrating a rapid thermal process chamber;

FIG. 2 is a functional block diagram of a system for detecting wafer fragments in a rapid thermal process chamber;

FIG. 3 is a cross-sectional side view of a viewing chamber for analyzing a wafer with a system for backside illumination of the wafer;

FIG. 4 is an exploded view of a viewing chamber as shown in FIG. 3;

FIG. 5 is a perspective view of a viewing assembly forming part of a viewing chamber as shown in FIG. 3;

FIG. 6 is a top view of a viewing assembly forming part of a viewing chamber as shown in FIG. 3;

FIG. 7 is a perspective view of an illumination shield forming part of a viewing chamber as shown in FIG. 3;

FIG. 8 is a top view of a wafer having a fragmented edge;

FIG. 9 is a flow diagram illustrating a technique for detecting wafer fragments in a rapid thermal process chamber;

FIG. 10 is a side view of a viewing chamber incorporating an alternative backside illumination system; and

FIG. 11 is a top view of a wafer with a backside illumination system as shown in FIG. 10.

Like reference numbers and designations in the various drawings indicate like elements.

DETAILED DESCRIPTION

FIG. 1 is a side view of a rapid thermal process chamber 10. As shown in FIG. 1, chamber 10 includes a bottom wall 12, opposing side walls 14, 16, top wall 18, and front and back walls (not shown in FIG. 1). Walls 12, 14, 16, and 18 enclose a heat source 20, a wafer support 22, and a reflector plate 24. FIG. 1 further illustrates a wafer 26 mounted in wafer support 22. Although a single wafer 26 is shown for purposes of example, rapid thermal process chamber 10 may be designed for the processing of two or more wafers. Chamber 10 may include other conventional equipment commonly used in rapid thermal processing applications. Such equipment may include, for example, pump equipment for evacuating chamber 10, gas distribution lines for delivery of process gas into the chamber, and various fixtures for supporting heat source 20 and reflector plate 24.

Heat source 20 may take the form of a flood lamp source or, as shown in FIG. 1, an array of lamp sources 28. Lamp sources 28 can be arranged in a two-dimensional array and individually controlled to allow zoned heating of the surface of wafer 26. An example of a rapid thermal processing system incorporating spatially zoned lamp sources is disclosed in United States Patent No. 5,155,336 to Gronet et al., the entire content of which is incorporated herein by reference. Each lamp source 28 can be fixtured within a reflective zone to concentrate heat onto wafer 26. Heat generated by heat source 20 is absorbed by wafer 26 during processing. Reflector

plate 24 forms a reflective cavity to reflect heat back onto wafer 26 and provide more effective heating.

To facilitate control of heat source 20, chamber 10 further includes a temperature sensing device. For example, chamber 10 may include one or more temperature sensor probes 30 that sense temperature at different positions across wafer 26. Two sensor probes 30 are illustrated in FIG. 1 for ease of illustration. Sensor probes 30 may take the form of pyrometers that transduce infrared radiation emitted by wafer 26 into temperature signals. An example of such a temperature measurement system is disclosed in United States Patent No. 5,660,472 to Peuse et al., the entire content of which is incorporated herein by reference. Alternatively, chamber 10 could incorporate an infrared camera, discrete thermocouples, thin film thermocouples, or other temperature sensing devices appropriate for measurement of temperature across the surface of wafer 26. The use of pyrometer-based sensor probes 30 will be described herein.

The temperature signals generated by sensor probes 30 can be fed back to a controller (not shown) that adjusts the intensities of individual lamp sources 28 to produce a desired spatial heating profile and thereby minimize thermal gradients across the surface of wafer 26. Each sensor probe 30 can be mounted adjacent a lower surface 31 of reflector plate 24 or, as shown in FIG. 1, integrated with the reflector plate. In either case, sensor probes 30 detect infrared radiation emitted from wafer 26 mounted on wafer support member 22. Each sensor probe 30 is positioned to monitor temperature within a particular area of wafer 26. An array of sensor probes 30 can be provided to span the entire surface area of wafer 26. In many applications, however, disposition of sensor probes 30 within certain sub-sections of reflector plate 24, or with irregular patterns, may provide information sufficient for the temperature control function, particularly for zoned lamp sources exhibiting a predetermined spatial heating profile for a given application.

During the rapid thermal process, fragments can break away from wafer 26, and fall onto areas, such as the top surface of reflector plate 24, positioned

between the wafer processing position and temperature sensor probes 30. The wafer fragments generally result from thermal gradients at the outer edge of wafer 26. Unfortunately, the wafer fragments can compromise the accuracy of the temperature signals generated by sensor probes 30, especially when the fragments fall onto reflector plate 24 at positions generally coincident with the probes. In particular, the fragments can land at positions between sensor probes 30 and wafer 26, interfering with the temperature signal received by the probes. This fragment-induced interference can attenuate or otherwise corrupt the temperature measurement signal, and adversely affect the temperature control function across the surface of wafer 26.

Excessive temperature gradients occur in the absence of effective temperature control. Such gradients can damage wafer 26, reducing device yield and degrading device quality. Also, the effects of the wafer fragments can persist for subsequent wafers processed within chamber 10 unless the fragment is cleared away from reflector substrate 24. In other words, a wafer fragment that breaks away from a single wafer could result in damage to an entire process run involving many subsequent wafers. To alleviate the potential effects of wafer fragments, in accordance with an embodiment of the present invention, a system for detection of wafer fragments is provided.

FIG. 2 is a functional block diagram of a system 32 for detecting wafer fragments in rapid process chamber 10. As shown in FIG. 2, system 32 includes an image acquisition device such as a charge coupled device (CCD) camera 34, an illumination source 36, a processor 38, and a memory 40. System 32 also may include a controller 42 that is responsive to an advisory generated by processor 38 to halt the operation of rapid thermal process chamber 10. Camera 34 is oriented to capture an image of a wafer 26 processed within chamber 10. Camera 34 can be positioned to acquire an image while wafer 26 is within rapid thermal processing chamber 10. In one embodiment, however, camera 34 is oriented to acquire an image of wafer 26 following exit of the wafer from chamber 10.

For example, camera 34 can be mounted on a viewing chamber in which wafer 26 is received upon exit from chamber 10. The viewing chamber can be formed by adaptation of a wafer cooling chamber. In this manner, the viewing chamber forms both an area for analysis of wafer 26 and cooling of the wafer prior to further processing. As a result, analysis can proceed without affecting the throughput of the rapid thermal process. Camera 34 can be mounted to a viewing port in the cooling chamber and oriented to capture a substantial portion of wafer 26 within its field of view. The image may take the form of a top view of wafer 26. Accordingly, camera 34 can be positioned above wafer 26, or coupled via optics components to receive a top view of the wafer.

Processor 38 analyzes the image acquired by camera 34 to detect the absence of a portion of the wafer by identifying an optical density contrast change, and determining whether a portion of the wafer is absent based on identification of the optical density contrast change. A contrast area on the surface of wafer 26 can be identified by comparing the optical density of the area to a target range of optical density. Data representative of the target range can be stored in memory 40 as density range data. Alternatively, processor 38 can be configured to compare successive pixels in the image for a predetermined density difference.

Proceeding on a pixel-by-pixel basis, for example, areas on wafer 26 in which no wafer fragment is missing will yield a given range of optical density. In those areas in which a wafer fragment is missing, however, the pixels will exhibit a different range of optical density. Thus, by analyzing contrast changes along a line or several lines of pixels, the potential presence of a wafer fragment can be detected. The analysis can proceed by logging subsequent pixels following the contrast change until another contrast change is detected. In this manner, the length or width of a potential fragment can be determined. Again, the contrast changes can be logged within a pixel line or column and between adjacent lines or columns to quantify the size of the individual wafer fragment, e.g., in terms of a length, width, or surface area. If the size

of the area exhibiting a different optical density is substantial and exceeds a predetermined threshold, presence of a wafer fragment on wafer 26 is indicated.

In other words, the size of the contrast area can be estimated, e.g., by counting the number of pixels occupying the contrast area, and the estimated size can be compared to a threshold value indicative of a fragment size large enough to affect the temperature measurement and control function of rapid thermal process chamber 10. If the estimated size exceeds the threshold value, the detection of the absence of a portion of the wafer, i.e., a wafer fragment, is indicated. The threshold can be determined by experimentation to exclude false positive detection results, particularly in light of perspective distortion, varying reflectivity due to differing fragment shape, and illumination variations within the chamber. In many cases, it may be desirable to allow the user to set the threshold according to a desired level of sensitivity and intervention. It may be necessary to recalibrate the threshold used in the fragment detection process for changing conditions within process chamber 10.

If desired, the threshold can be set not only for a single contrast area, but for a cumulative contrast area. In this case, the threshold may correspond to a total number of contrasting pixels across the surface of the wafer that, together, are indicative of the potential presence of a fragment or fragments that could undermine the temperature control function. For example, whereas a single fragment may have a size insufficient to appreciably alter the temperature measurement function, the cumulative effect of a number of fragments could be undesirable. Thus, processor 38 may compare the size of an individual fragment to a threshold, or simply sum the contrasting pixels across the portion of the wafer surface analyzed and compare the sum to a cumulative threshold.

Upon indication of a wafer fragment, processor 38 generates an advisory as the basis for automatic or manual intervention to halt operation of the rapid thermal process. The advisory can be communicated to an operator for human intervention or, optionally, to controller 42. Controller 42 automatically intervenes in the rapid thermal process workflow. For example, controller 42 can halt the rapid thermal

process for manual or automated cleaning of reflector plate 24 prior to insertion of the next wafer into chamber 10. If desired, the advisory also may include information indicating the estimated size and number of any wafer fragments for consideration by the operator or for logging to a file for later analysis. This information also may convey the position of the wafer fragment, at least along one dimension of wafer 26. All of the above information can be communicated to the user in graphic and/or text format. Also, if desired, a monitor can be provided to enable an operator to view the acquired image.

To facilitate identification of a contrast area within the acquired image, wafer 26 preferably is set against an illuminated background surface. In this case, the target range of optical density corresponds to a range of optical density exhibited by the illuminated background surface. To enhance the contrast analysis, the background surface can be illuminated about the edge portion of wafer 26 with a ring-like pattern of illuminating radiation to thereby provide back-illumination for the wafer. In the event a wafer fragment is missing, the back-illumination shows through the missing area of the wafer for ease of identification by processor 38.

To project the ring-like pattern of illuminating radiation and substantially prevent incidence of the radiation on the top surface of wafer 26, an illumination shield can be used. The illumination shield defines an interior region and an exterior region, and is oriented such that the illuminating radiation projected by the illumination source is substantially restricted to the exterior region and a field of view of the image acquisition device is substantially restricted to the interior region. Also, the exterior region is arranged such that the illuminating radiation illuminates a portion of the background surface adjacent an edge portion of wafer 26 to thereby provide back-illumination while avoiding illumination of the top surface of the wafer.

To minimize image processing, the portion of the acquired image corresponding to the edge of wafer 26 can be analyzed while discarding the remainder of the image. Wafer fragments are most prevalent at the edge of the wafer. Therefore, analysis of the edge of wafer 26 ordinarily will be sufficient for

identification of potential wafer fragments. In this manner, the necessary image processing can be undertaken in a more economical manner, with a focus on those portions of wafer 26 known to be most susceptible to fragmentation. With analysis limited primarily to the edge portion, back-illumination of only the edge portion is sufficient for effective contrast analysis. Hence, the ring-like pattern of light provides effective illumination.

FIG. 3 is a cross-sectional side view of a viewing chamber 46 for analyzing a wafer 26. FIG. 4 is an exploded view of viewing chamber 46. As shown in FIGS. 3 and 4, viewing chamber 46 includes a base 48 and a main housing 50. As shown in FIG. 3, viewing chamber 46 also includes a viewing assembly 52. Base 48 may include a side port 54 for receipt of wafer 26 within a support area 56. Wafer 26 can be transferred into side port 54 using a conventional wafer transfer mechanism such as a transfer blade. Viewing chamber 46 can be integrated with a cooling chamber. Accordingly, base 48 can take the form of a cooling block, and may therefore include appropriate fittings and internal conduits for the flow of coolant. Wafer 26 is supported within support area 56 above a background surface 58 by a wafer mount structure (not shown). The wafer mount structure may include, for example, conical quartz rods having points that contact the wafer. The rods can be mounted into machined holes in base 48. Base 48 further includes an aperture 59 with a mounting lip 60 for receipt of a bottom mounting flange 62 of main housing 50. Mounting flange 62 can be coupled to mounting lip 60 with, for example, bolts 64. Main housing 50 has a generally cylindrical sidewall 66 and houses a conically-shaped illumination shield 68. Illumination shield 68 can be suspended above wafer 26 and within aperture 59 by machined brackets (not shown). The brackets can be attached to base 48 at points along the periphery of aperture 59.

With further reference to FIGS. 3, 4, 5, and 6, viewing assembly 52 includes an image acquisition device in the form of a camera 72, and an illumination source that may take the form of a light ring 74. Light ring 74 defines a central aperture 76. A lens portion 77 of camera 72 extends through central aperture 76 and

is separated by light ring 74 by a collar 78. As particularly shown in FIG. 4, main housing 50 defines an upper aperture 80 and an upper mounting lip 82. A mounting ring 84 mounts to mounting lip 82 with bolts 85, and defines a recess 86 for receipt of a transparent viewing plate 87. The viewing plate separates camera 72 and light ring 72 from vapors within main housing 50. A camera mount 88 fastens onto an upper surface 90 of main housing 50 via bolts 92. Camera 72 is securely mounted to camera mount 88 with screws 94, and via a bracket 95, and oriented to view downward into the interior of main housing 50. Handles 96, 98 are also mounted to upper surface 90 of main housing 50, e.g., with bolts 100, to facilitate installation and removal of viewing assembly 52.

With particular reference to FIG. 3, illumination shield 68 defines an interior region 102 and an exterior region 104. Illumination shield 68 has a substantially conical shape, with a first substantially circular opening 106 having a first diameter and a second substantially circular opening 108 having a second diameter. The second opening 108 is defined by a cylindrical portion 110 of illumination shield 68. FIG. 7 shows illumination shield 68 mounted within aperture 59 of base 48. Second opening 108 of illumination shield 68 is sized slightly larger than the size of wafer 26. In particular, the diameter of second opening 108 is slightly larger than and concentric with the diameter of wafer 26. Illumination shield 68 and viewing assembly 52 are oriented such that the ring-like pattern of illuminating radiation generated by light ring 74 is not directly incident on a top surface of wafer 26. Instead, as shown in FIG. 3, the illuminating radiation is generally restricted to exterior region 104, and is incident on background surface 58 proximate to an edge portion 112 of wafer 26. In this manner, the illuminating radiation is incident on background surface 58 to provide back-illumination for wafer 26, but is not incident on a top surface of the wafer. At the same time, the field of view of camera 72 is generally restricted to interior region 102, and therefore does not receive the illuminating radiation projected by light ring 74.

To prevent incidence of the illuminating radiation on a top surface of wafer 26, illumination shield 68 is made from a substantially opaque material that blocks the emission of radiation into interior region 102. At the same time, the exterior surface of illumination shield 68 and the interior surface of main housing 50 can be made substantially reflective to allow propagation of the illuminating radiation with less attenuation, e.g., somewhat like a light pipe. Also, the diameter of second opening 108 is sized to allow the ring-like pattern of radiation to project downward to background surface 58 slightly outside of the diameter of wafer 26. The radiation incident on background surface 58 is reflected upward, however, substantially enhancing the optical contrast between intact portions of wafer 26 and any fragmented portion through which the back-illumination is visible.

To provide a uniform pattern of back-illumination, light ring 74 preferably provides a diffuse pattern of light. Also, background surface 58 can be structured, if desired, to reflect illuminating radiation more diffusely. Lens portion 77 of camera 72 is positioned concentrically with first opening 106, and views only the upper surface of wafer 26. Specifically, the field of view of camera 72 is substantially blind to stray illuminating radiation projected by light ring 74. In this manner, illumination shield 68 is capable of significantly enhancing the contrast analysis performed by processor 38 to identify potential wafer fragments. Contrast can be further enhanced by adjusting the height of wafer 26 within chamber 46 and relative to base 48, for example, with a wafer lift pin mechanism provided in the chamber. Also, a dark ring can be formed on the inner surface of cylindrical portion 110 to eliminate back reflections. Such a dark ring could be formed by an aluminum ring that is hard black anodized and riveted in place.

FIG. 8 is a top view of a wafer 26 having a fragmented edge. As shown in FIG. 8, wafer 26 is set against background surface 58 for contrast analysis. In operation, processor 38 analyzes an image of wafer 26, as acquired by camera 72, on a pixel-by-pixel basis to identify contrast changes. In the example of FIG. 8, processor 38 would observe an edge portion 112, one section of which has a contrast area

corresponding to a fragment portion 114 of wafer 26. In particular, processor 38 identifies the contrast area by comparing the optical density of the area to a target range of optical density associated with background surface 58. For example, whereas the surface of wafer 26 will exhibit a generally uniform optical density, or at least an optical density with a given range fragment portion 114 will exhibit an optical density commensurate with the illuminating radiation reflected by background surface 58. In most cases, the illuminating radiation should be intense enough to provide a distinct contrast between wafer 26 and background surface 58. In particular, the difference in optical density should be sufficient to counteract optical disparities that can lead to nonuniformities in the acquired image.

As further shown in FIG. 8, the image acquired by camera 72 can be processed by processor 38 to discard a substantial portion and retain merely an edge portion 112. Specifically, processor 38 can effectively discard a central portion 116 from consideration in the contrast analysis. Central portion 116 can be discarded in recognition that wafer fragments are most prevalent at edge portion 112. Accordingly, to avoid undue processing overhead, processor 38 can be configured to focus on the region in which wafer fragments are most prevalent. From experience, the user may adjust the size of the edge portion 112 under analysis, or optionally undertake an analysis of the entire surface of wafer 26. In most cases, however, analysis of edge portion 112 will be sufficient for identification of wafer fragments that could adversely affect the temperature measurement and control function. As an example, analysis of an edge band having a width of approximately 2 mm ordinarily will be sufficient to identify potentially problematic wafer fragments.

Also, in some applications, it will be sufficient that only a section of edge portion 112 be analyzed. With reference to FIG. 1, for example, sensor probes 30 can be positioned within a sub-section of reflector plate 24, rather than across the entire surface area of plate 24 consistent with the spatial temperature profile of heat source 20. Consequently, the analysis of only those portions of wafer 26 that correspond to positions of sensor probes 30 on reflector plate 24 may be sufficient to identify the

wafer fragments that are most likely to impact the accuracy of the temperature signals generated by the probes. In this case, other wafer fragments could be excluded from consideration as being less detrimental to the temperature control function. In many cases, however, it may be desirable to identify wafer fragments, without regard to impact on the temperature control function, in order to detect defective wafers. In the event that the positions of sensor probes 30 extend over a larger area of reflector plate 24, however, processor 38 may consider that larger area. Also, it should be recognized that wafer fragments can fall on different areas of the reflector plate as wafer 26 is removed from chamber 10.

FIG. 9 is a flow diagram illustrating a technique for detecting wafer fragments in a rapid process chamber. As shown in FIG. 9, processor 38 drives camera 72 and illumination source 74 to acquire an image of wafer 26 within viewing chamber 46, as indicated by block 118. If desired, camera 72 could acquire the actual image prior to exit of wafer 26 from rapid thermal process chamber 10, e.g., by providing an appropriate optics path for camera 72 to view the wafer. In many cases, however, a view of wafer 26 within rapid thermal process chamber 10 will be obscured. Accordingly, it ordinarily will be desirable to capture the wafer image following exit, e.g., in the cooling chamber. Following acquisition of the image of wafer 26, in this embodiment, processor 38 discards the center portion and retains the portion corresponding to the wafer edge, as indicated by block 120. As indicated by block 122, processor 38 then analyzes the acquired image for optical density contrast changes. Processor 38 next quantifies either the overall size of the contrast regions or the sizes of individual regions, as indicated by block 124. Processor 38 then determines whether the size exceeds a predetermined threshold, as indicated by block 126. If so, processor 38 generates an advisory and optionally halts the rapid thermal process for the next wafer until the wafer fragment is cleared, as indicated by blocks 128 and 130. If the size does not exceed the threshold, processor 38 generates no advisory and the rapid thermal process continues, as indicated by block 132.

FIG. 10 is a side view of an alternative viewing chamber 134. Viewing chamber 134 conforms substantially to viewing chamber 46 of FIG. 3. Accordingly, like reference numerals are used throughout FIGS. 3 and 10 to denote similar structure. In contrast to viewing chamber 46, however, viewing chamber 134 incorporates an alternative backside illumination system for wafer 26. Specifically, whereas viewing chamber 46 makes use of light ring 74 and illumination shield 68 mounted in an upper area of the chamber, viewing chamber 134 incorporates a light ring 136 mounted in a recessed area 138 within base 48. Thus, as shown in FIG. 10, light ring 136 is disposed below wafer 26 to thereby provide direct backside illumination from a side opposite the image acquisition device. In particular, light ring 136 emits illuminating radiation upward against the backside 140 of wafer 26. Light ring 136 can be covered by a quartz window 142 that is also provided in recessed area 138. Also, a suitable electrical feedthrough can be formed in base 48 to provide electrical power to light ring 136.

FIG. 11 is a top view of wafer 26 in conjunction with light ring 136. As shown in FIG. 11, light ring 136 is sized and positioned to overlap an edge portion 144 of wafer 26. Wafer 26 substantially blocks a portion of the illuminating radiation from transmission to camera 72. However, a portion of the illuminating radiation outside of edge portion 144 of wafer 26 is visible by camera 72, thereby enhancing optical density contrast at the edge. In this manner, intact areas of wafer 26 appear relatively dark relative to fragmented areas or areas outside of edge portion 144, which allow transmission of the backside illumination provided by light ring 136 to camera 72. In the event a fragment breaks away from the edge portion of wafer 26, as indicated by reference numeral 146, the optical contrast provided by light ring 136 facilitates fragment identification using machine vision techniques as described above.

A contrast analysis, as described herein, can be implemented using well known machine vision techniques and commercially available systems for executing them. For example, machine vision systems capable of implementing contrast analysis techniques are available from Cognex Corporation of Natick, Massachusetts.

An example of a suitable machine vision system is the Cognex MVS 8000 Series system, which includes a set of PC-based machine vision hardware and software tools. With such a system, the images can be analyzed on a pixel-by-pixel basis to evaluate optical density differences. If the optical density differs by more than a threshold value, the pixel can be recorded as a contrasting pixel.

In light of the commercial availability of systems generally dedicated to machine vision applications, in the implementation of a contrast analysis, processor 38 may take the form of any conventional general purpose single- or multi-chip microprocessor such as a Pentium® processor, a Pentium Pro® processor, an 8051 processor, a MIPS processor, a Power PC® processor, or an Alpha® processor. Alternatively, processor 38 may take the form of a special purpose microprocessor embedded within a dedicated machine vision system. In the exemplary Cognex MVS 8000 Series system described above, processor 38 may be a Pentium® processor with the MMX instruction set. In any event, processor 38 executes program code arranged to carry out conventional image processing for the analysis of optical contrast comparison of the actual and reference images. As a further alternative, processor 38 could take the form of a custom logic circuit arranged to execute a wafer fragment detection process as described herein.

Camera 72 may take the form of a two-dimensional CCD pixel array having lateral and vertical fields of view that span multiple pixels. In this manner, the acquired images provide multiple pixel rows and columns for quantification of both the widths and lengths of fragments for comparison to a threshold value, such as pixel count. Thus, an overall deviation threshold value can be established by reference to a total number of contrasting pixels in the image. Alternatively, contrasting pixels can be grouped according to proximity within adjacent columns and rows, thereby quantifying the overall cross-sectional size of individual wafer fragments. In this case, the deviation threshold value is established with respect to a maximum size tolerance for wafer fragments. Light ring 74 or 136 may take the form of a fiber

optic-based ringlight, such as those commercially available from Fostec, of Auburn, New York, and especially configured for machine vision and microscopy applications.

The foregoing detailed description has been provided for a better understanding of the invention and is for exemplary purposes only. Modifications may be apparent to those skilled in the art without deviating from the spirit and scope of the appended claims.

WHAT IS CLAIMED IS:

1. A system for analysis of a wafer for the absence of wafer fragments, the system comprising:

a viewing chamber;

a wafer support member disposed within the chamber;

an illumination source that generates back-illuminating radiation for a wafer positioned on the wafer support member; and

an image acquisition device oriented to acquire an image representative of at least an edge portion of the wafer.

2. The system of claim 1, further comprising a background surface, wherein the illumination source is disposed on a side of the wafer opposite the background surface, the system further comprising an illumination shield disposed within the viewing chamber, the illumination shield defining an interior region and an exterior region, wherein the illumination shield is oriented such that the illuminating radiation generated by the illumination source is substantially restricted to the exterior region and a field of view of the image acquisition device is substantially restricted to the interior region, and the exterior region is arranged such that the illuminating radiation illuminates a portion of the background surface adjacent the edge portion of the wafer to thereby provide back-illuminating radiation for the edge portion of the wafer.

3. The system of claim 2, wherein the illumination shield has a substantially conical shape, the illumination shield including a first substantially circular opening having a first diameter and a second substantially circular opening having a second diameter, wherein the second opening is sized larger than the size of the wafer supported in the wafer support area such that the illuminating radiation generated by the illumination source light source is not directly incident on a top

surface of the wafer but is incident on the background surface proximate to the edge portion of the wafer.

4. The system of claim 3, wherein the illumination source projects a substantially ring-like pattern of illuminating radiation.

5. The system of claim 4, wherein the illumination source has a substantially ring-like shape defining a central aperture, the image acquisition device having a field of view that extends through the central aperture.

6. The system of claim 5, wherein the image acquisition device and the illumination source are disposed adjacent one another, and the image acquisition device has a lens that extends through at least a portion of the central aperture, the illumination source extending around a periphery of the lens.

7. The system of claim 1, wherein the illumination source is disposed on a side of the wafer adjacent the background surface and opposite the image acquisition device.

8. The system of claim 7, wherein the illumination source projects a substantially ring-like pattern of illuminating radiation toward a side of the wafer adjacent the background surface.

9. The system of claim 8, wherein the substantially ring-like pattern of illuminating radiation overlaps the edge portion of the wafer.

10. The system of claim 1, further comprising a processor that analyzes the acquired image to detect the absence of a portion of the wafer, and generates an advisory in the event the absence of a portion of the wafer is detected.

11. The system of claim 10, wherein the processor analyzes the acquired image by identifying an optical density contrast change, and determines whether a portion of the wafer is absent based on identification of the optical density contrast change.

12. The system of claim 11, wherein the processor is configured to analyze the acquired image by identifying a contrast area having an optical density that contrasts with a target range of optical densities, estimating a size of the contrast area, comparing the estimated size to a threshold value, and indicating detection of the absence of a portion of the wafer in the event the estimated size exceeds the threshold value.

13. The system of claim 10, further comprising a controller that halts operation of the rapid thermal process chamber in response to generation of the advisory by the processor.

14. The system of claim 10, wherein the viewing chamber forms an integral portion of a cooling chamber.

15. The system of claim 10, wherein the processor is further configured to analyze the acquired image by identifying a contrast area along the edge portion of the wafer having an optical density that contrasts with a range of optical densities exhibited by back-illuminating radiation, estimating the size of the contrast area, comparing the estimated size to a threshold value, and indicating detection of the absence of a portion of the wafer in the event the estimated surface area exceeds the threshold value.

16. A system for detecting the presence of a wafer fragment in a deposition process chamber, the system comprising:

an illumination source that provides back-illuminating radiation about an edge portion of a wafer processed within the chamber;

an image acquisition device oriented to acquire an image representative of at least the edge portion of the wafer; and

a processor that analyzes the acquired image to detect the absence of a portion of the wafer, and generates an advisory in the event the absence of a portion of the wafer is detected.

17. The system of claim 16, wherein the processor analyzes the acquired image by identifying an optical density contrast change, and determines whether a portion of the wafer is absent based on identification of the optical density contrast change.

18. The system of claim 16, wherein the processor is configured to analyze the acquired image by identifying a contrast area having an optical density that contrasts with a target range of optical densities, estimating a size of the contrast area, comparing the estimated size to a threshold value, and indicating detection of the absence of a portion of the wafer in the event the estimated size exceeds the threshold value.

19. The system of claim 18, wherein the processor identifies the contrast area by identifying a plurality of adjacent pixels having optical densities in a common range of optical densities different than the target range of optical densities.

20. The system of claim 19, wherein the processor estimates the size of the contrast area by counting a number of the adjacent pixels within the contrast area, and indicates detection of the absence of a portion of the wafer in the event the counted number of adjacent pixels exceeds a threshold pixel count value.

21. The system of claim 18, wherein the illumination source provides back-illuminating radiation for the edge portion of the wafer relative to the image acquisition device, and wherein the target range of optical densities corresponds to a range of optical densities exhibited by the back-illuminating radiation.

22. The system of claim 16, further comprising a controller that halts operation of the rapid thermal process chamber in response to generation of the advisory by the processor.

23. The system of claim 16, wherein the image acquisition device is oriented to acquire the image after the wafer has been removed from the rapid thermal process chamber.

24. The system of claim 23, wherein the image acquisition device is oriented to acquire the image following receipt of the wafer within a cooling chamber.

25. The system of claim 24, further comprising a viewport disposed above a position at which the wafer is received within the cooling chamber, wherein the image acquisition device is oriented to acquire the image as a top view image of the wafer via the viewport.

26. The system of claim 23, further comprising an illumination shield defining an interior region and an exterior region, the illumination shield being oriented such that the illuminating radiation projected by the illumination source is substantially restricted to the exterior region and a field of view of the image acquisition device is substantially restricted to the interior region, the exterior region being arranged such that the illuminating radiation illuminates a portion of a background surface adjacent the edge portion of a wafer to thereby provide the back-illuminating radiation for the edge portion of the wafer.

27. The system of claim 26, wherein the processor is further configured to analyze the acquired image by identifying a contrast area along the edge portion of the wafer having an optical density that contrasts with a range of optical densities exhibited by the background surface during the illumination, estimate the size of the contrast area, compare the estimated size to a threshold value, and indicate detection of the absence of a portion of the wafer in the event the estimated size exceeds the threshold value.

28. The system of claim 23, wherein the illumination source is disposed on a side of the wafer adjacent the background surface and opposite the image acquisition device.

29. A method for detecting the presence of a wafer fragment in a deposition process chamber, the method comprising:

illuminating an area adjacent an edge portion of a wafer processed within the chamber;

acquiring an image representative of at least a portion of the wafer, wherein the illuminating radiation provides back-illuminating radiation for the edge portion of the wafer;

analyzing the acquired image to detect the absence of a portion of the wafer; and

generating an advisory in the event the absence of a portion of the wafer is detected.

30. The method of claim 29, further comprising analyzing the acquired image by identifying an optical density contrast change, and determining whether a portion of the wafer is absent based on identification of the optical density contrast change.

31. The method of claim 29, further comprising analyzing the acquired image by:

identifying a contrast area having an optical density that contrasts with a target range of optical densities;

estimating a size of the contrast area;

comparing the estimated size to a threshold value; and

indicating detection of the absence of a portion of the wafer in the event the estimated size exceeds the threshold value.

32. The method of claim 31, further comprising identifying the contrast area by identifying a plurality of adjacent pixels having optical densities in a common range of optical densities different than the target range of optical densities.

33. The method of claim 32, further comprising estimating the size of the contrast area by counting a number of the adjacent pixels within the contrast area, and indicating detection of the absence of a portion of the wafer in the event the counted number of adjacent pixels exceeds a threshold pixel count value.

34. The method of claim 31, wherein the target range of optical densities corresponds to a range of optical densities exhibited by the back-illuminating radiation.

35. The method of claim 29, further comprising halting operation of the rapid thermal process chamber in response to generation of the advisory.

36. The method of claim 29, further comprising acquiring the image after the wafer has been removed from the rapid thermal process chamber.

37. The method of claim 36, further comprising acquiring the image following receipt of the wafer within a cooling chamber.

38. The method of claim 37, wherein the cooling chamber includes a viewport disposed above a position at which the wafer is received within the cooling chamber, and the act of acquiring the image includes acquiring a top view image of the wafer via the viewport.

39. The method of claim 38, further comprising analyzing the acquired image by:

identifying a contrast area along the edge of the wafer having an optical density that contrasts with a range of optical densities exhibited by the background surface during the illumination;

estimating the size of the contrast area;

comparing the estimated size to a threshold value; and

indicating detection of the absence of a portion of the wafer in the event the estimated surface area exceeds the threshold value.

40. The method of claim 29, wherein the act of acquiring an image includes providing an illumination shield defining an interior region and an exterior region, and orienting the illumination shield such that the illuminating radiation projected by the illumination source is substantially restricted to the exterior region and a field of view of the image acquisition device is substantially restricted to the interior region, the exterior region being arranged such that the illuminating radiation illuminates a portion of the background surface adjacent the edge of the wafer to thereby provide the back-illuminating radiation for the edge of the wafer.

41. The method of claim 40, further comprising analyzing the acquired image by identifying a contrast area along the edge of the wafer having an optical density that contrasts with a range of optical densities exhibited by the background surface during the illumination, estimating the size of the contrast area, comparing the estimated size to a threshold value, and indicating detection of the absence of a portion of the wafer in the event the estimated surface area exceeds the threshold value.

42. The method of claim 37, wherein the act of illuminating includes illuminating the wafer from a side of the wafer opposite the image acquisition device.

43. The method of claim 42, further comprising analyzing the acquired image by identifying a contrast area along the edge of the wafer having an optical density that contrasts with a range of optical densities exhibited by the background surface during the illumination, estimating the size of the contrast area, comparing the estimated size to a threshold value, and indicating detection of the absence of a portion of the wafer in the event the estimated surface area exceeds the threshold value.

44. A system for analysis of a wafer for the absence of wafer fragments, the system comprising:

a viewing chamber;

a wafer support member disposed within the chamber;

an illumination that generates back-illuminating radiation about an edge portion of the wafer; and

an image acquisition device oriented to acquire an image representative of at least an edge portion of a wafer positioned on the wafer support member.

45. The system of claim 44, wherein the illumination source projects a substantially ring-like pattern of illuminating radiation.

46. The system of claim 44, further comprising a processor that analyzes the acquired image to detect the absence of a portion of the wafer, and generates an advisory in the event the absence of a portion of the wafer is detected.

47. A system for analysis of a wafer for the absence of wafer fragments, the system comprising:

a viewing chamber;

a wafer support member disposed within the chamber;

a background surface disposed adjacent the wafer support member within the viewing chamber;

an image acquisition device oriented to acquire an image representative of at least an edge portion of a wafer positioned on the wafer support member from a side of the wafer support member opposite the background surface;

an illumination source that projects illuminating radiation within the viewing chamber;

an illumination shield disposed within the viewing chamber, the illumination shield defining an interior region and an exterior region, wherein the illumination shield is oriented such that the illuminating radiation is substantially restricted to the exterior region and a field of view of the image acquisition device is substantially restricted to the interior region, and the exterior region is arranged such that the illuminating radiation illuminates a portion of the background surface adjacent an edge of the wafer to thereby provide back-illuminating radiation for the edge of the wafer.

48. The system of claim 47, wherein the illumination shield has a substantially conical shape, the illumination shield including a first substantially circular opening having a first diameter and a second substantially circular opening having a second diameter, wherein the second opening is sized larger than the size of a wafer supported in the wafer support area such that the illuminating radiation generated by the illumination source light source is not directly incident on a top surface of the wafer but is incident on the background surface proximate to an edge of the wafer.

49. A system for analysis of a wafer for the absence of wafer fragments, the system comprising:

a viewing chamber;

a wafer support member disposed within the chamber;

means for providing back-illumination of a side of a wafer positioned on the wafer support member; and

an image acquisition device oriented to acquire an image representative of at least an edge portion of the wafer, the image acquisition device acquiring a portion of the back-illumination in the event a wafer fragment is absent from the edge portion of the wafer.

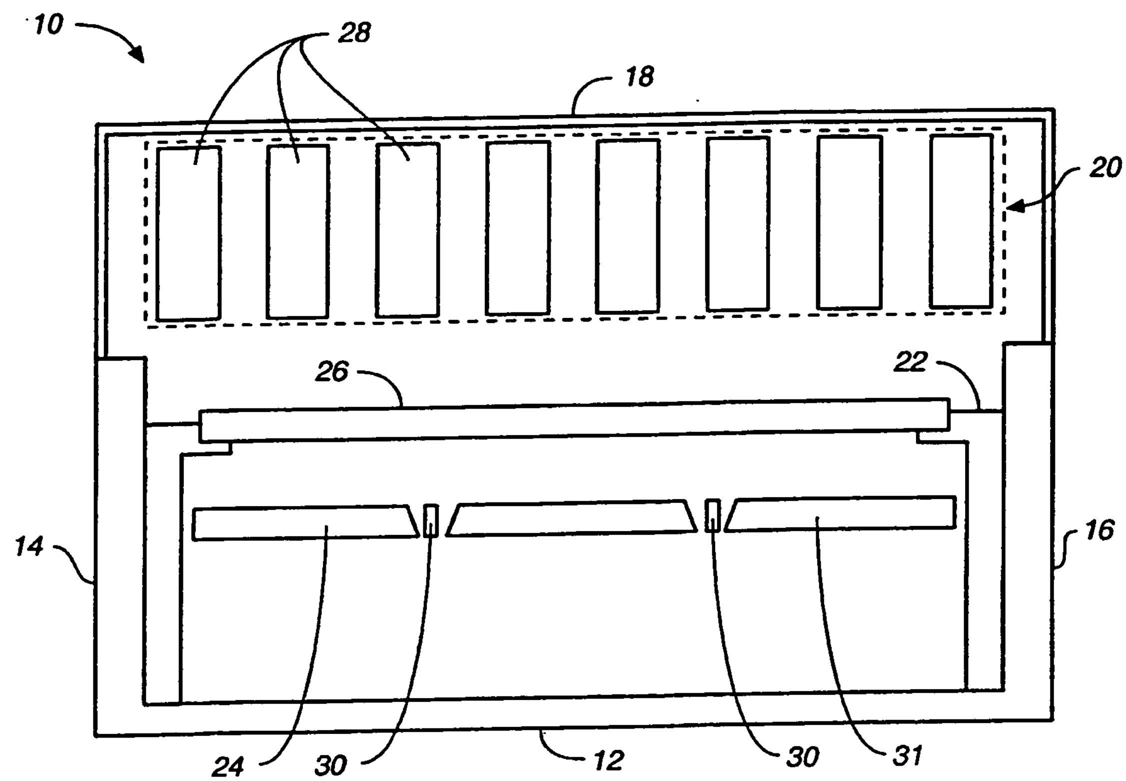
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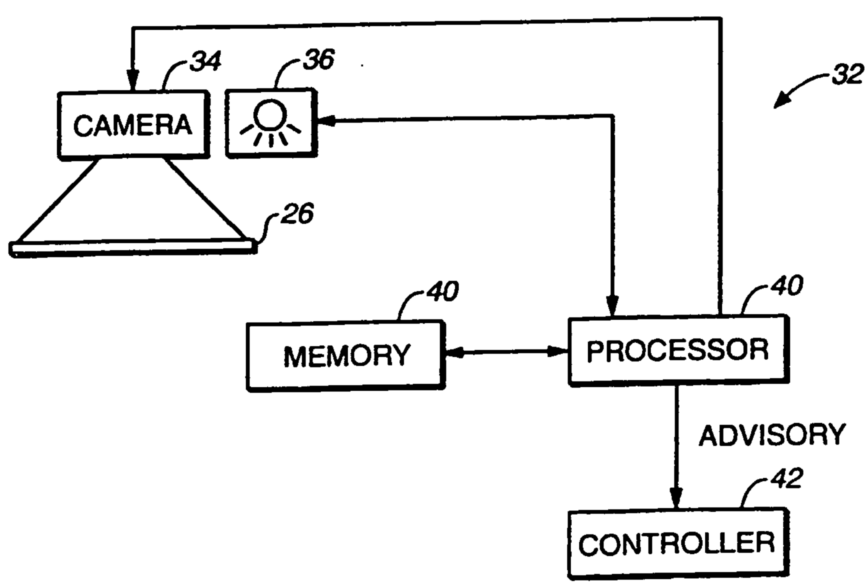
FIG._1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CONTROLLER

FIG._2

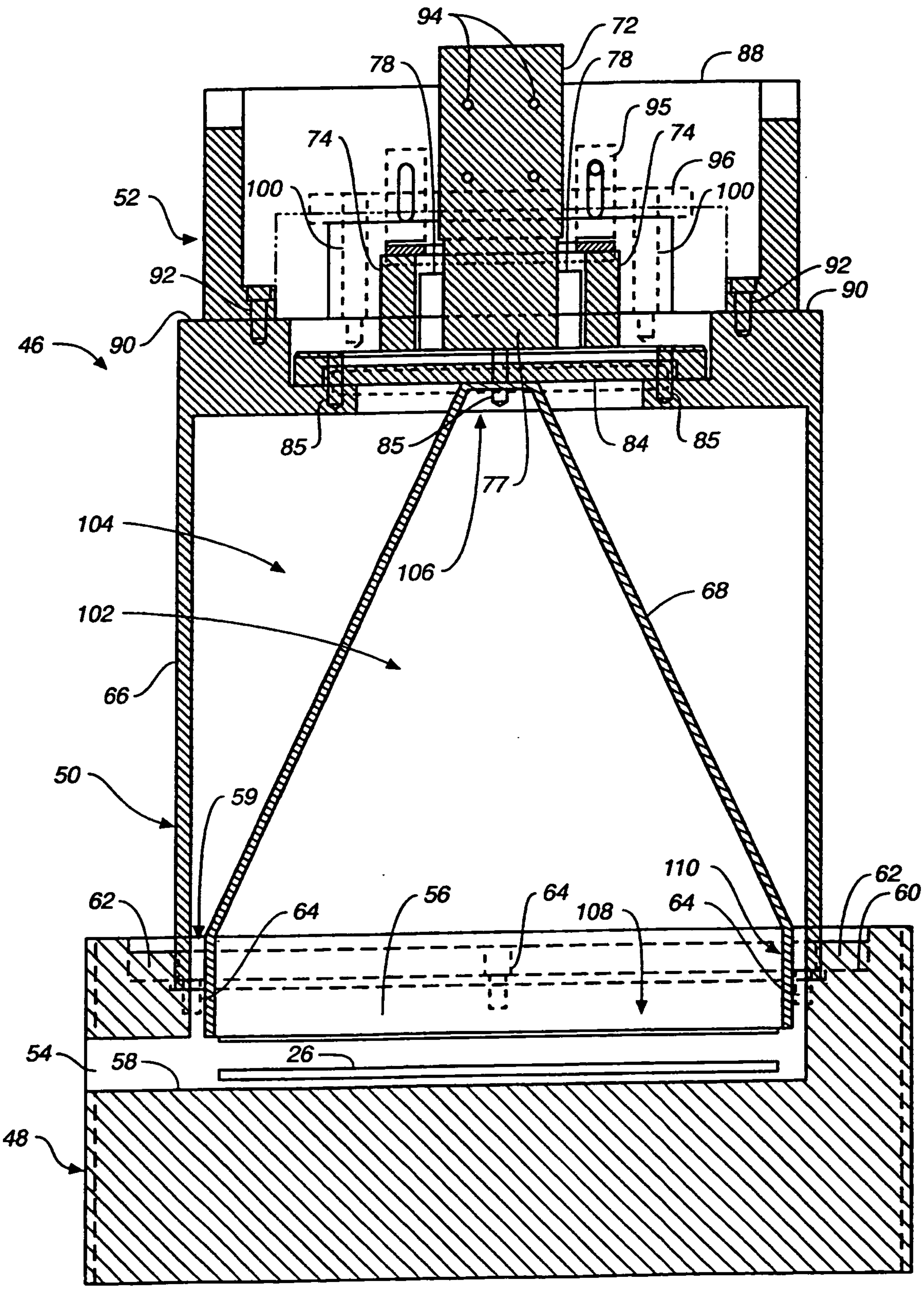
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FIG._3

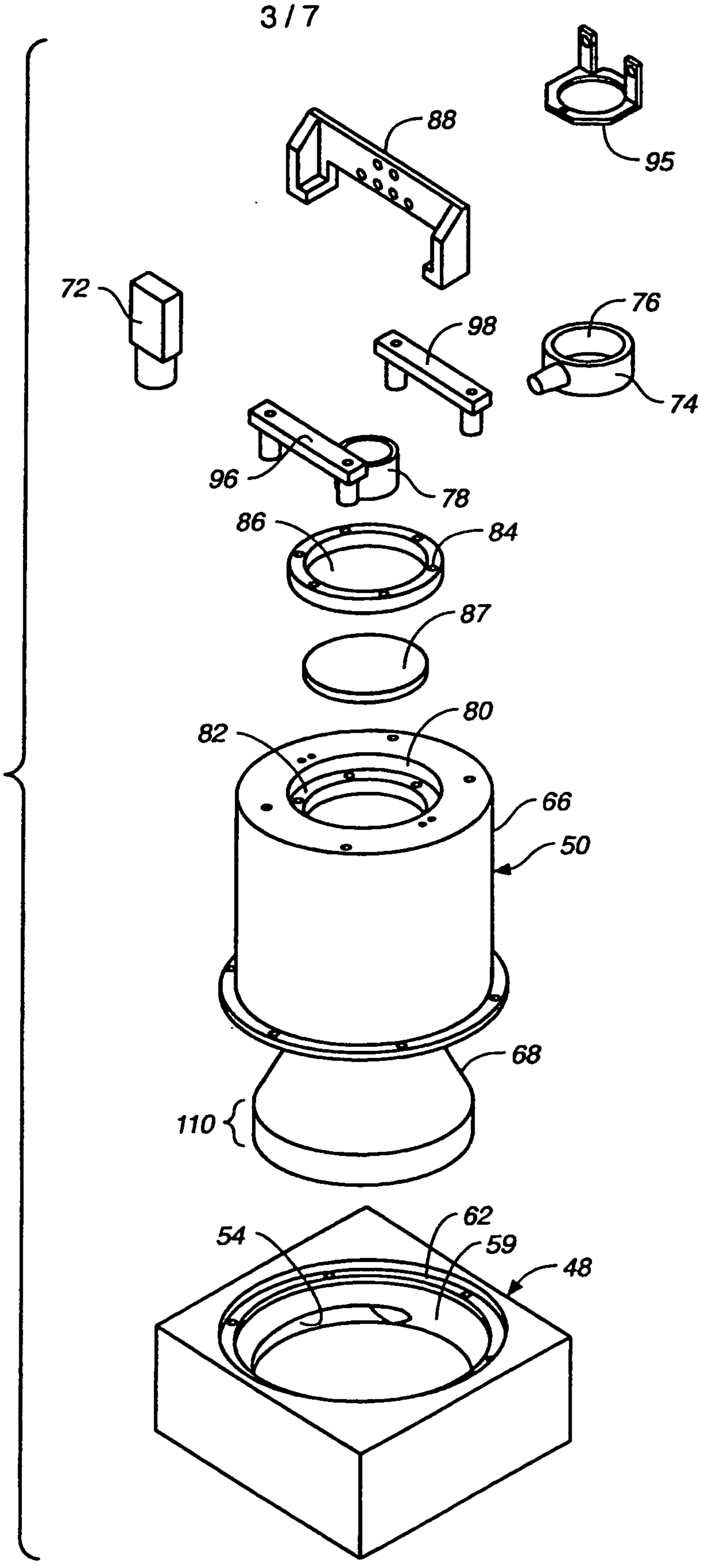


FIG._4

FIG._5

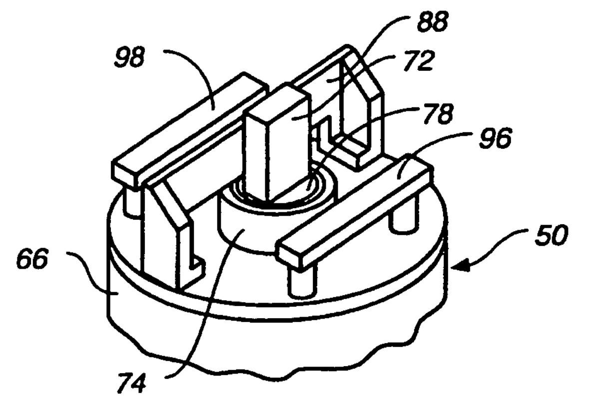


FIG._6

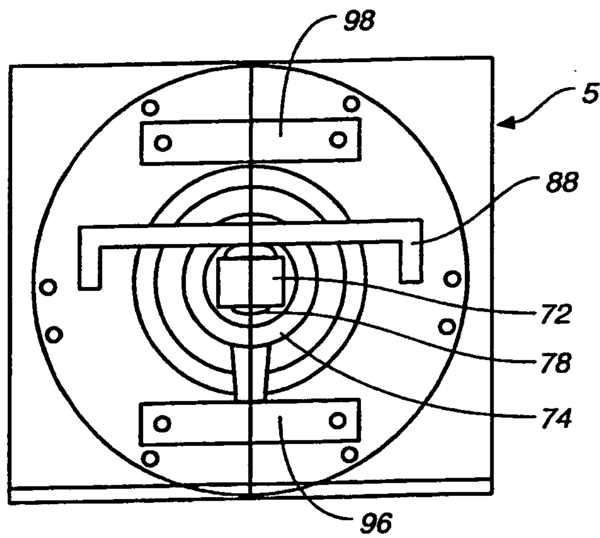


FIG._7

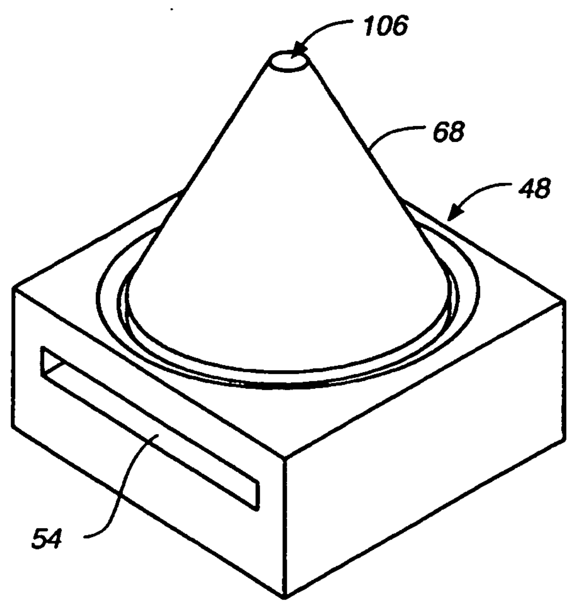


FIG._8

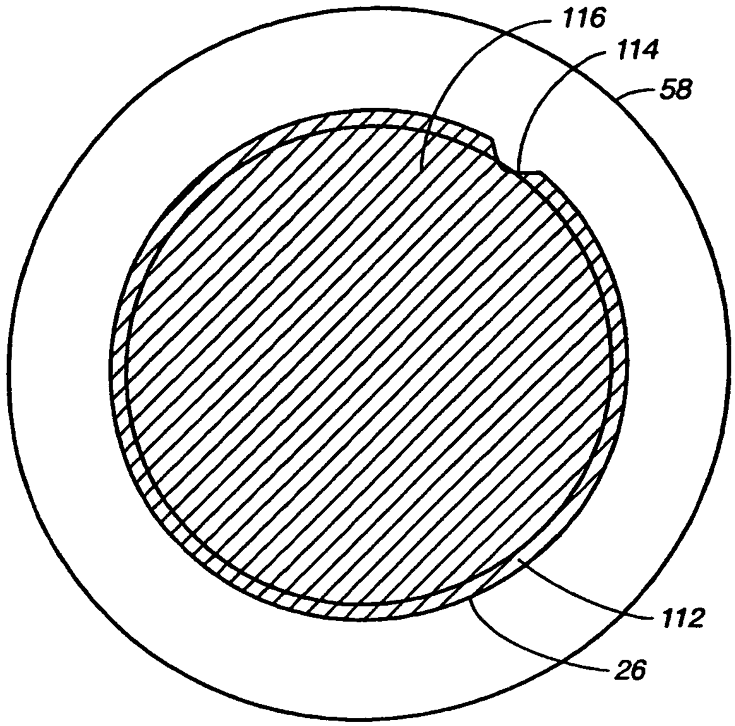
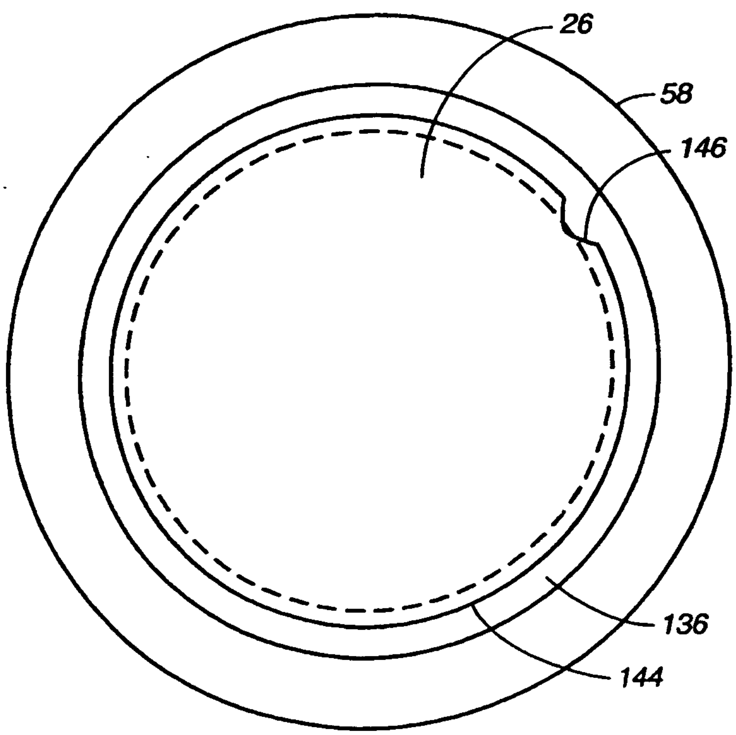


FIG._11



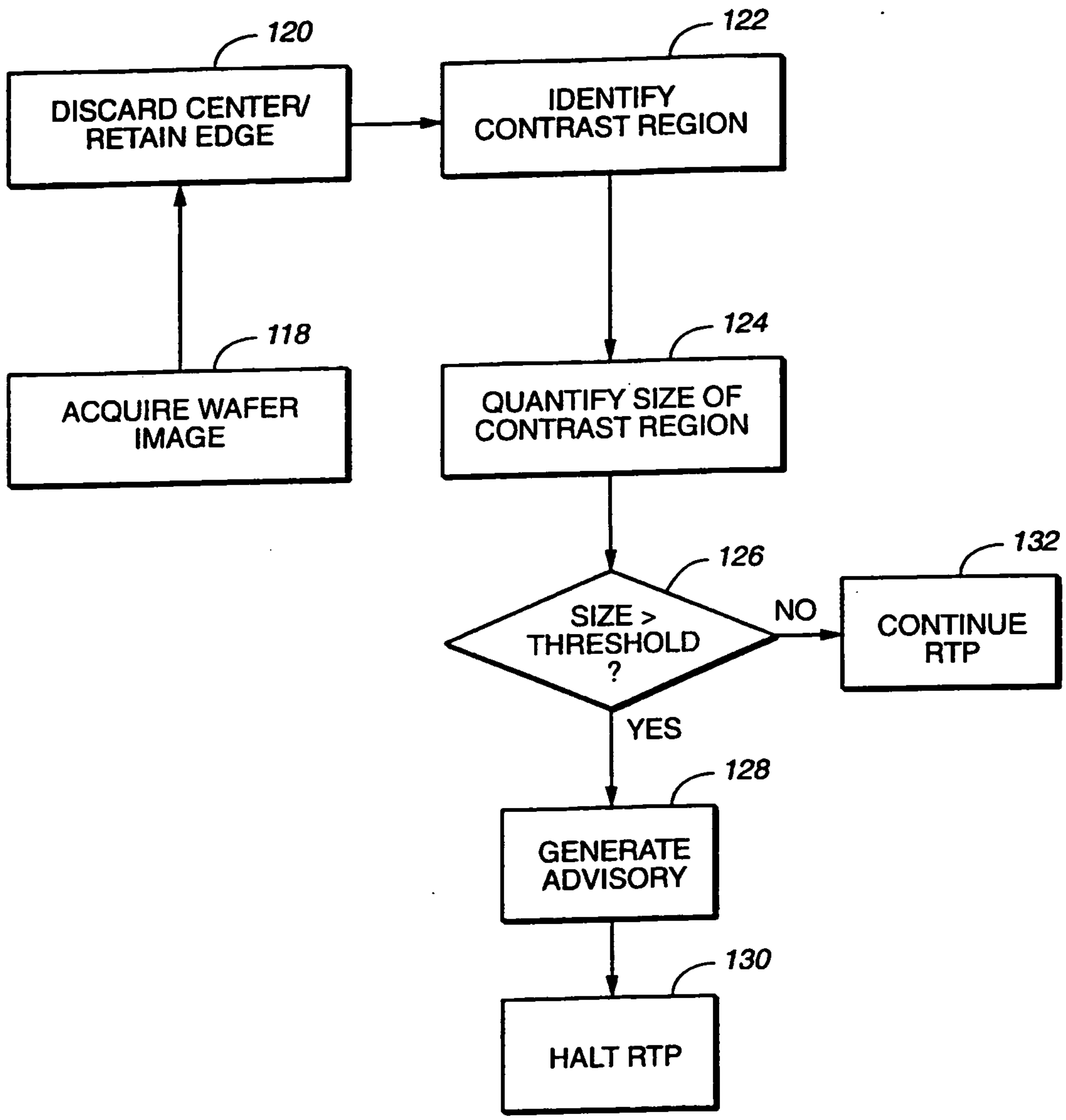

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FIG._9

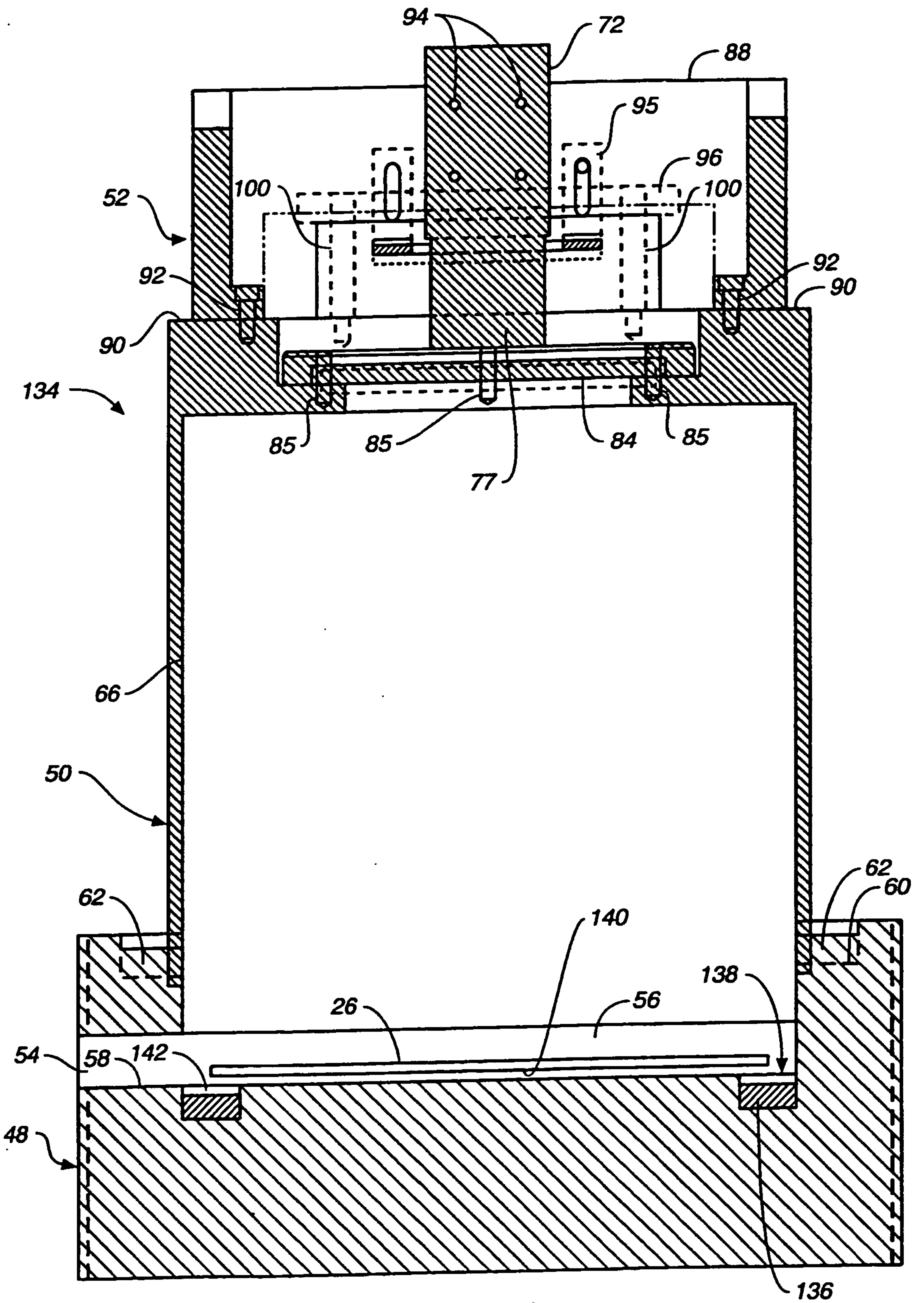
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FIG._10

INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 99/24382

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/00

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	PATENT ABSTRACTS OF JAPAN vol. 1997, no. 05, 30 May 1997 (1997-05-30) -& JP 09 016779 A (ASIA ELECTRON INC), 17 January 1997 (1997-01-17) abstract	1,16,29, 44,47,49
A	US 5 745 594 A (MIYAHARA) 28 April 1998 (1998-04-28) abstract	1,16,29, 44,47,49
A	WO 97 21189 A (COGNEX CORPORATION) 12 June 1997 (1997-06-12) page 19, line 1-12	1,16,29, 44,47,49
A,P	US 5 962 862 A (EVERS ET AL.) 5 October 1999 (1999-10-05) column 4, line 49-65	1,16,29, 44,47,49

☐ Further documents are listed in the continuation of box C.

☒ Patent family members are listed in annex.

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"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
1 March 2000	08/03/2000

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL – 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Oberle, T

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INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/US 99/24382

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